REMARKS

Claims 20, 22, 24-29 and 31 are pending in this application. Claims 20, 26 and 28 are independent claims.

In the Advisory Action dated February 21, 2003, the Examiner maintains the final rejection of claims 20, 22 and 24-29 and 31 under 35 USC §103(a) as being obvious over Katchmar (U.S. Patent No. 6,194,782 B1). It is respectfully submitted that the amendment herein of independent claims 20, 26 and 28 serves to distinguish the claimed invention over Katchmar.

In the Final Action, dated September 6, 2002, the Examiner points to Katchmar as teaching a semiconductor device, Figures 1-5, comprising: a substrate 12 having a main surface 14 and a back surface 16, wherein said back surface 16 has a central area 32, an intermediate area without any solder bumps surrounding said central area 32 (see included red marked by the Examiner, copy of Figure 5) and a peripheral area surrounding said intermediate area; a semiconductor chip 18 formed on said main surface; a first bump unit formed of solder bumps 40, Figure 5, disposed at a first distance from each other and located in said central area of said back surface, wherein said first bump unit radiates heat from said semiconductor device; a second bump unit formed of solder bumps 24 and located in said peripheral area of said back surface, wherein said second bump unit transmits signals (column 6, lines 50-53), wherein the second bump unit is greater in quantity of solder balls than the first bump unit, and said solder balls are spherical in shape. Further, the Examiner asserts that Katchmar teaches a first distance between connection solder balls being greater than a second distance between heat transfer solder balls (column 7, lines 39-47). Further yet, the Examiner points to Figures 1-4 of Katchmar as teaching that said central area could be thermally connected to said circuit board by a solid melted solder mass 26.

However, the Examiner acknowledges that Katchmar fails to teach that the second distance is less than a width of the intermediate area (i.e., the distance between the central area and the peripheral area), as required by independent claims 20 and 26. Regarding the intermediate area, the Examiner refers to a marked-up copy of Katchmar Figure 5 to show the various areas and distances recited in the claims. Attached to this document is the figure from Katchmar that the Examiner had earlier marked up. Applicant has further

added letters "c" and "d" to the figure to designate the width of the intermediate area marked by the Examiner, and the distance between the bumps of the second bump unit, respectively. It is evident that the width of the intermediate area, c, in Katchmar is less than the distance between the bumps in the peripheral area, d.

While the Examiner contends that the space between the bumps in the central area and the bumps of the peripheral area corresponds to the intermediate area recited in the claims, it is respectfully submitted that there is nothing about that space to distinguish it from the peripheral area or to indicate that it is not simply part of the peripheral area itself. There is nothing disclosed in the text of Katchmar to suggest an intermediate area at all; only that the solder balls under the semiconductor die (i.e., in the central area) are placed in closer proximity to each other than those not positioned under the die (i.e., in the peripheral area) (see column 7, lines 42-44).

In short, it is respectfully submitted that the Examiner's argument in the Final Action, while attempting to identify an intermediate area in Katchmar, does not demonstrate a distinct intermediate area having a width greater than the distance between the bumps of the second bump unit, as the claims require.

To emphasize the distinction between the claimed invention and Katchmar, each of claims 20, 26 and 28 is amended to recite that "said back surface has ..., a distinct intermediate area in which no bumps are disposed, surrounding the central area" (emphasis added). The amended language finds support in Figures 1-3 of the application. The changes to the claims are shown in the Appendix, with deletions indicated by bracketing and additions by underlining.

In the Final Action, the Examiner also acknowledges Katchmar fails to teach that the melted solder mass can be made by locating bumps of the first bump unit sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body; and that the first distance is about 1 to 1.4 times the diameter of the bumps of the first bump unit, and the second distances about 1.6 to 1.7 times the diameter of the bumps in the second bump unit (claim 31). To overcome this defect in Katchmar, the Examiner argues that it would have been an obvious matter of design choice to make the first distance sufficiently small that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body; or

making the first distance about 1 to 1.4 times the diameter of the bumps of the first bump unit, and the second distance about 1.6 to 1.7 times the diameter the bumps of the second bump unit, since such a modification would have involved a mere change in the size of a component. The Examiner invokes *In re Rose*, 105 USPQ 237 (CCPA 1995) for the principle that change in size is generally recognized as being within the level of ordinary skill in the art. The Examiner asserts that the applicant has not shown that these particular ranges of sizes are critical by showing that the claimed range achieves unexpected results relative to the prior art range, citing *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934, (Fed. Cir. 1990), as support.

It is respectfully submitted that the present invention is not, as the Examiner suggests, simply a case of establishing an appropriate bump spacing in the central area as a matter of design choice. The claims recite a functional limitation, namely "the bumps of the first bump unit are sufficiently close to each other that upon application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body," that fundamentally distinguishes the present invention over Katchmar. Katchmar discloses two different embodiments for improving heat flow away from the semiconductor chip in the central area of the substrate. Figures 1-4 discloses a single solder mass 26 that replaces the solder balls in the area under the semiconductor chip 18, and only that area (column 6, line 66 through column 7, line 1). In Figure 5, a plurality of closely spaced solder balls 40 replaces the single solder mass 26 under the semiconductor chip (column 7, lines 39-48). The two methods are discussed in Katchmar strictly in the alternative (column 7, lines 44-47). Nowhere does Katchmar disclose or suggest placing these solder balls in the central area sufficiently close together that they fuse into a unitary body when heat treatment is applied to mount the device package to a printed circuit board. Quite the contrary, Figures 5-7 clearly show the substrate mounted to the printed circuit board with individual solder balls. Placing the solder balls closer together in the central area does not inherently lead to their fusing together when heated.

In short, while Katchmar recognizes the benefit of spacing the solder balls more closely together under the semiconductor chip than in the peripheral area, to improve heat transfer, it totally fails to suggest the further benefits to be realized by placing the solder

balls sufficiently close that they fuse into a unitary mass when heated to bond the substrate to a circuit board.

In the Advisory Action, the Examiner argues that when designing a chip and accordingly, its solder balls (bumps) for connecting to a circuit board, one of the main concerns is to avoid (prevent) short circuiting of the solder balls (a "collapse," as it is known in the art). The Examiner asserts that there are many well-known ways in the art to achieve that. For example, one of them is to "fan out" the terminals of the chip, which means to increase distances between solder balls. Alternatively failing to do this will inherently lead to melting solder balls together. The Examiner does not see any reason to consider such an outcome as a patentable novelty for an apparatus claim.

It is respectfully submitted that the teaching to which Examiner refers is applicable to the peripheral area in which it is desirable to prevent adjacent signal leads from shorting together when the solder balls are heated and reflow to attach the semiconductor assembly to a printed circuit board. That much is disclosed in the present application. However, while the phenomenon of solder balls shorting when they are placed too close together may be known, neither Katchmar nor the art cited by the Examiner suggests the advantage, in terms of the resulting heat flow efficiency, of spacing solder ball so close together that they fuse into a unitary body when heated. Further the invention advantageously allows the same size solder balls to be used both in the central area and in the peripheral area when the semiconductor device is being fabricated. This reduces manufacturing cost and time as compared to procuring and attaching a separate solder mass for heat conduction, as in Katchmar (e.g., item 26 of Katchmar Figure 4).

All of the claim rejections having been addressed, it is respectfully submitted that the application, as amended, is in condition for allowance. Notice of such, with allowed claims 20, 22, 24-29 and 31, is earnestly solicited.

[Continued next page]

Should the Examiner believes that an interview would be helpful in resolving any open issues regarding this application, the Examiner is respectfully invited to call the undersigned attorney to schedule of such an interview.

Respectfully submitted,

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Date

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Appendix
Attachment

APPENDIX

AMENDMENTS TO CLAIMS

(Deletions indicated by bracketing and additions by underlining)

20. (Thrice Amended) A semiconductor device, comprising:

a substrate having a main surface and a back surface,

wherein said back surface has a central area, [an] a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding said intermediate area;

a semiconductor chip disposed on said main surface;

a first bump unit disposed in said central area of said back surface,

wherein said first bump unit includes a plurality of bumps that are disposed a first distance apart from each other, and

wherein said first bump unit radiates heat from said semiconductor device; and

a second bump unit formed in said peripheral area of said back surface,

wherein said second bump unit includes a plurality of bumps that are disposed a second distance apart from each other, said second distance is greater than said first distance, and said second distance is less than a third distance between said central area and said peripheral area, and

wherein said second bump unit transmits signals.

26. (Twice Amended) A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, [an] a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed on the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other, the second distance being greater than the first distance and less than a third distance between the central area and the peripheral area,

wherein the first and second distances are set such that upon application of a heat treatment to the device, the bumps of the first bump unit melt so as to become connected and fuse to each other as a unitary body and the bumps of the second bump unit melt and remain apart from each other.

28. (Four Times Amended) A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, [an] a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed on the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other sufficient to assure that upon application of a heat treatment to the device causing the bumps of the first and second bump units to melt, the bumps of the second bump unit remain apart from each other, the second distance being greater than the first distance and less than a width of the intermediate area;

wherein the bumps of the first bump unit are sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body.

ATTACHMENT A

Katchmar

$b > a$

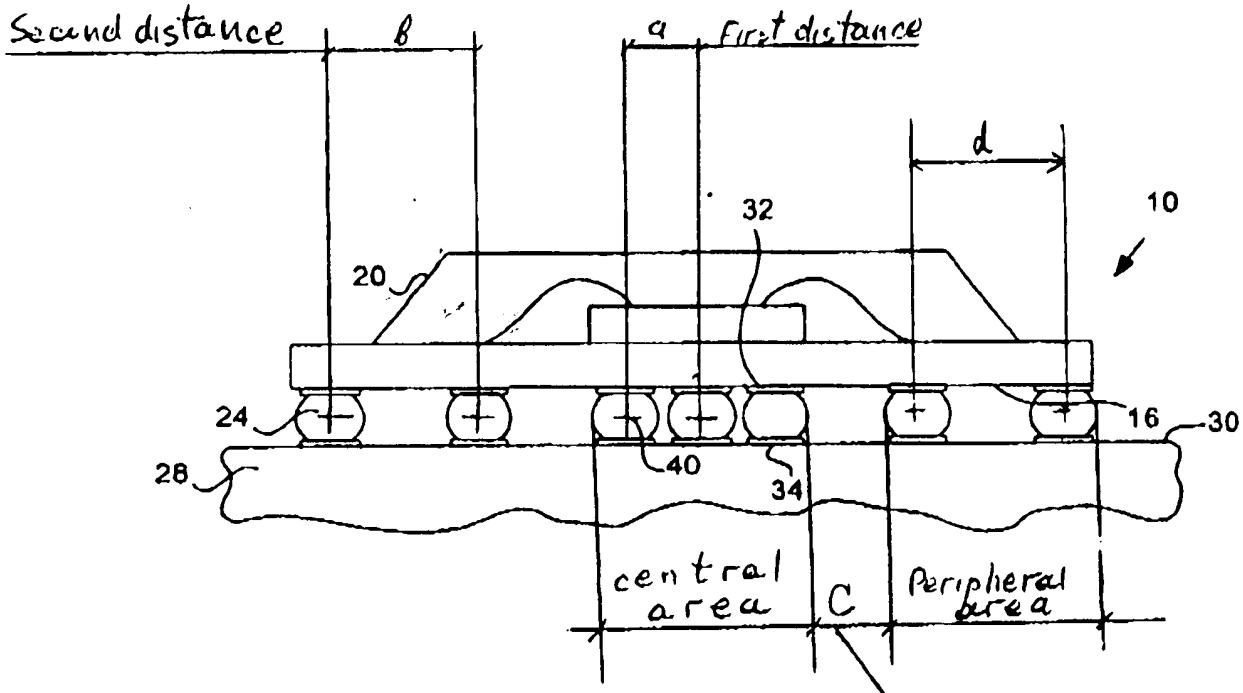

Fig. 5

$c < d$